



Platinum Coated Si Wafers:

Description:

The **Platinum Coated Silicon Wafers** (where Platinum coating acting as Bottom Electrode) starts with a silicon wafer having **half a micron (0.5 μ)** of thermally grown silicon dioxide on its surface. The customer may specify the wafer type for purchase by Vin Karola or the customer may supply the wafers. Otherwise, the process generally uses 500 μ thick <100> or <111> boron doped silicon wafers, one side polished with a typical resistivity of 1-10 Ohm-cm.

The first deposit is a **400 \AA** layer of Titanium dioxide (TiO₂) on the surface of the Silicon dioxide (SiO₂) followed by **1500 \AA** of pure Platinum (Pt). The platinum is not patterned.

The top surface of the silicon wafer may be **Silicon nitride instead of Silicon dioxide**. As well, the customer may elect to supply wafers having other mechanical features in or under the silicon surface. The primary requirement is that the surface of the wafer be Silicon dioxide or Silicon nitride.

Substrates other than standard silicon wafers may be used. Process has successfully deposited the Platinum/PNZT stack on both sides of double-side polished quartz wafers. Thin silicon wafers may also be used in place of the standard 500 μ thick silicon wafers but allowances must be made for breakage during processing.

The typical Platinum coated Silicon wafers have the following specs.

Silicon Wafer (Platinized)

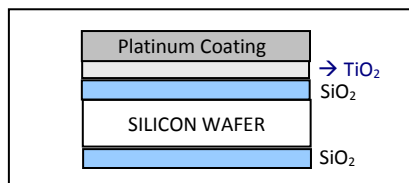
Orientation <100> or <111> Prime Grade

Size: 100mm dia x ~500u thick

P-type/Boron doped with thermally grown SiO₂ surface

Deposit Layers:

1. Silicon Dioxide (SiO₂) 0.5 μ (both sides of wafer)
2. Titanium Dioxide (TiO₂) 400 \AA \pm 50 \AA (Polished side)
3. Platinum (Pt) 1500 \AA \pm 100 \AA (Polished side)
(Typical Pt resistivity: 15 μ Ohm-cm)



These wafers are typically used for the deposition and growth of **thin ferroelectric films** from sputtered sources or spin-on solutions *in an oxidizing atmosphere*. Sintering temperatures typically reach 650C to 850C and the stress change during sintering is tremendous, reaching hundreds of gigapascals of tension or compression before reducing again. Typical ferroelectric film stress after completion is about 100 gigapascals of tension. The platinum historically will not rip off and does not grow hillocks during the stress changes of ferroelectric film crystallization. The platinum will begin to develop small cracks above 750C due to differences in the coefficients of thermal expansion between the platinum and the silicon so we recommend that users remain below 750C when depositing thin films on these wafers.

Research and Development Products

